WHAT IS CLAIMED IS:

1. A transceiver, comprising:
multiple parallel ports;
multiple serial ports; and
a bus connecting said multiple parallel ports and said multiple serial ports on a common substrate with said multiple parallel ports and said multiple serial ports.

2. The transceiver of claim 1, wherein said bus is configured to have a ring shape.

3. The transceiver of claim 1, wherein said bus is configured to have a ring shape around a logic core.

4. The transceiver of clam 1, further comprising a packet bit error rate tester (BERT) connected to said bus, said packet BERT able to determine bit error rates of at least one of said multiple parallel ports and said multiple serial ports.

5. The transceiver of claim 1, wherein said multiple parallel ports include two parallel ports and said multiple serial ports includes four serial ports.

6. The transceiver of claim 1, wherein said multiple parallel ports are XGMII parallel ports.

7. The transceiver of claim 1, wherein said multiple serial ports are XAUI serial ports.

8. The transceiver of claim 1, wherein said serial ports convert between a XAUI serial protocol and a XGMII parallel protocol using a XGXS conversion protocol.

9. The transceiver of claim 1 wherein said bus is a parallel bus.

10. The transceiver of claim 9, wherein said parallel bus includes multiple transmission lines having a common path length.

11. The transceiver of claim 9, wherein each of said serial ports include a serial-to-parallel converter, a parallel port of said serial-to-parallel converter connected to said parallel bus.

12. The transceiver of claim 1, further comprising at least one management pad, said management pad able to determine data protocols and electricals for said transceiver.

13. The transceiver of claim 12, wherein said management pad is responsive to two or more protocols.

14. The transceiver of claim 13, wherein said two or more protocols include an IEEE Std 802.3 clause 22 management standard and an IEEE Std 802.3 clause 45 management standard.

15. The transceiver of claim 12, wherein said management pad is responsive to a data protocol of a first type of standard, and an electrical protocol of a second type of standard.

16. The transceiver of claim 15, wherein said first type of standard is one of an IEEE Std 802.3 clause 45 standard and an IEEE Std 802.3 clause 22 standard, and said second type of standard is the other of said IEEE Std 802.3 clause 45 standard and said IEEE Std 802.3 clause 22 standard.

17. The transceiver of claim 1, wherein data clock rates of said serial data ports and said parallel data ports are programmable.

18. The transceiver of claim 1, wherein said multiple serial data ports and said multiple parallel data ports can be enabled and disabled to provide a specific configuration for said transceiver.

19. The transceiver of claim 18, wherein two of said multiple serial data ports are enabled.

20. The transceiver of claim 19, wherein at least one of said multiple serial ports is disabled.

21. The transceiver of claim 18, wherein at least one of said multiple parallel ports is enabled.

22. The transceiver of claim 21, wherein at least one of said multiple parallel ports is disabled.

23. The transceiver of claim 1, further comprising at least one custom logic block connected to said bus.

24. The transceiver of claim 18, further comprising a configuration block that enables and disables said multiple parallel ports and said multiple serial ports to configure said transceiver.

25. The transceiver of claim 24, wherein said configuration block also determines defaults of said transceiver.